

## CLAIMS

What is claimed is:

- 1           1.       A method of allocating a trace array from a cache memory, comprising:  
2       dividing said cache memory into a reduced-size cache memory and a trace array;  
3       permitting storage of trace signal data into said trace array; and  
4       permitting retrieval of said trace signal data from said trace array.
- 1           2.       A method as defined in Claim 1 wherein said reduced-size cache memory  
2       is equal in size to said trace array.
- 1           3.       A method as defined in Claim 1 wherein said reduced-size cache memory  
2       is not equal in size to said trace array.
- 1           4.       A method as defined in Claim 1 wherein said cache memory is 512K bytes  
2       in size.
- 1           5.       A method as defined in Claim 1 wherein at least one of said cache  
2       memory and said reduced-size cache memory is organized in eight-way associativities.
- 1           6.       A method as defined in Claim 1 wherein said cache memory comprises a  
2       directory array.
- 3           7.       A method as defined in Claim 6 wherein said directory array comprises an  
4       address field having a spare bit usable in a trace mode to represent a high order bit of a  
5       requested address.

1           8.       A method as defined in Claim 1, further comprising:  
2 detecting a trace mode.

1           9.       A method as defined in Claim 1 wherein said cache memory is comprised  
2 by a system-on-chip environment.

3           10.      A method as defined in Claim 1 wherein the combination of said  
4 reduced-size cache memory and said trace array comprises a split cache spanning the  
5 addressable space of said cache memory.

1           11.      A method as defined in Claim 1 wherein the permitted retrieval of said  
2 trace signal data from said trace array is configured as a broadside output from said trace  
3 array.

1           12.      A method as defined in Claim 1 wherein the permitted retrieval of said  
2 trace signal data from said trace array is configured as a compartmentally selected output  
3 from said trace array.

1           13.      A method as defined in Claim 1 wherein said reduced-size cache memory  
2 and said trace array are each associated with a separate output bus.

1           14.      A method as defined in Claim 1, further comprising:  
2 characterizing a self-timed interconnect using said trace array; and  
3 switching back to the original cache functionality once characterization is  
4 complete.

1           15.     A method as defined in Claim 14, further comprising:  
2                 at least one of multiplexing and time-sharing said self-timed interconnect signals  
3                 with other signals to be stored in said trace array.

1           16.     A storage medium encoded with a machine-readable computer program  
2                 code for allocating a trace array from an original cache memory, said storage medium  
3                 including instructions for causing a computer to implement a method comprising:  
4                     dividing the cache memory into a reduced-size cache memory and a trace array;  
5                     permitting storage of trace signal data into said trace array; and  
6                     permitting retrieval of said trace signal data from said trace array.

1           17.     A computer data signal for allocating a trace array from an original cache  
2                 memory, said computer data signal comprising code configured to cause a computer to  
3                 implement a method comprising:  
4                     dividing the cache memory into a reduced-size cache memory and a trace array;  
5                     permitting storage of trace signal data into said trace array; and  
6                     permitting retrieval of said trace signal data from said trace array.

1           18.     A cache memory comprising:  
2                 means for dividing said cache memory into a reduced-size cache memory and a  
3                 trace array;  
4                 means for permitting storage of trace signal data into said trace array; and  
5                 means for permitting retrieval of said trace signal data from said trace array.